Digital I/O
Parallel I/O

• Each pin in a parallel I/O port carries a single bit of information

• The port carries many bits of information in parallel

• Parallel I/O requires many data lines. Serial I/O requires few lines, but is slower (in a clock for clock comparison)

• The 68HC11 has five 8-bit parallel ports (configurable – Ports B and C can only be used for Parallel I/O)
The MCU (MicroController Unit)
Block Diagram of the 68HC11
Case 1
Polling I/O, no interrupt.
CPU must check a status bit to determine whether an I/O request occurred.

Case 2
Interrupt-driven I/O
I/O request causes interrupt and CPU responds to interrupt.

Figure 8.1 Generic I/O Subsystems
Memory Map

![Memory Map Diagram]

- $0000 - 256 bytes RAM
- $00FF - 64-byte register block
- $1000 - $103F
- $B000 - $B0FF
- $B040 - $B0FF
- $B000
- $E000 - 8 Kbytes ROM
- $FFFF - 512 bytes EEPROM
- $FFFF
- $FFFF
- Normal modes interrupt vectors
- Special modes interrupt vectors
Register and Control Bit addresses

<table>
<thead>
<tr>
<th>Address</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1000</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$1001</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$1002</td>
<td>STAF</td>
<td>STAI</td>
<td>CWOM</td>
<td>HNDS</td>
<td>OIN</td>
<td>PLS</td>
<td>EGA</td>
<td>INVB</td>
</tr>
<tr>
<td>$1003</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$1004</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$1005</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$1006</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$1007</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$1008</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$1009</td>
<td>Bit 5</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$100A</td>
<td>Bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bit 0</td>
</tr>
<tr>
<td>$100B</td>
<td>FOC1</td>
<td>FOC2</td>
<td>FOC3</td>
<td>FOC4</td>
<td>FOC5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$100C</td>
<td>OC1M7</td>
<td>OC1M6</td>
<td>OC1M5</td>
<td>OC1M4</td>
<td>OC1M3</td>
<td></td>
<td></td>
<td>OC1M</td>
</tr>
<tr>
<td>$100D</td>
<td>OC1D7</td>
<td>OC1D6</td>
<td>OC1D5</td>
<td>OC1D4</td>
<td>OC1D3</td>
<td></td>
<td></td>
<td>OC1D</td>
</tr>
</tbody>
</table>

- PORTA: I/O Port A
- Reserved
- PIOC: Parallel I/O Control Register
- PORTC: I/O Port C
- PORTB: Output Port B
- PORTCL: Alternate Latched Port C
- Reserved
- DDRC: Data Direction for Port C
- PORTD: I/O Port D
- DDRD: Data Direction for Port D
- PORTE: Input Port E
- CFORC: Compare Force Register
- OC1M: OC1 Action Mask Register
- OC1D: OC1 Action Data Register
Example

PORT B
$1004

<table>
<thead>
<tr>
<th>PB0</th>
<th>PB1</th>
<th>PB2</th>
<th>PB3</th>
<th>PB4</th>
<th>PB5</th>
<th>PB6</th>
<th>PB7</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Example: LDAA #$A5
STAA $1004

Case 1
Parallel Output

PORT C (configured as input)
$1003

<table>
<thead>
<tr>
<th>PC0</th>
<th>PC1</th>
<th>PC2</th>
<th>PC3</th>
<th>PC4</th>
<th>PC5</th>
<th>PC6</th>
<th>PC7</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Example: LDAA $1003
Then ACCA has the value $63

Case 2
Parallel Input
Ports

• Port A:
  – Data Register: $1000 (PORTA)
  – Three input pins (PA0-PA2), four output pins (PA3-PA6), one bidirectional pin (PA7)
  – Bit 7 in PACTL register ($1026) sets direction for PA7

• Port B:
  – Data Register: $1004 (PORTB)
  – Parallel outputs only
Ports 2

• Port C:
  – Data Register: $1003 (PORTC)
  – Parallel inputs or outputs
  – Direction configured by register DDRC ($1007)

• Port D:
  – Data Register: $1008 (PORTD)
  – Pins PD0 – PD5 are inputs or outputs (the rest are reserved)
  – Direction configured by register DDRD ($1009) (B0 – B5)

• Port E:
  – Data Register: $100A (PORTE)
  – Parallel inputs only
The 128-byte register block can be remapped to any 4K boundary.

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA7</td>
<td>PA6</td>
<td>PA5</td>
<td>PA4</td>
<td>PA3</td>
<td>PA2</td>
<td>PA1</td>
<td>PA0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>STA1</td>
<td>STA2</td>
<td>CWOM</td>
<td>HNDS</td>
<td>OIN</td>
<td>PL5</td>
<td>EGA</td>
<td>INV8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PIOC</td>
</tr>
<tr>
<td>PC7</td>
<td>PC6</td>
<td>PC5</td>
<td>PC4</td>
<td>PC3</td>
<td>PC2</td>
<td>PC1</td>
<td>PC0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTC</td>
</tr>
<tr>
<td>PB7</td>
<td>PB6</td>
<td>PB5</td>
<td>PB4</td>
<td>PB3</td>
<td>PB2</td>
<td>PB1</td>
<td>PB0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTB</td>
</tr>
<tr>
<td>PCL7</td>
<td>PCL6</td>
<td>PCL5</td>
<td>PCL4</td>
<td>PCL3</td>
<td>PCL2</td>
<td>PCL1</td>
<td>PCL0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTC</td>
</tr>
<tr>
<td>DDC7</td>
<td>DDC6</td>
<td>DDC5</td>
<td>DDC4</td>
<td>DDC3</td>
<td>DDC2</td>
<td>DDC1</td>
<td>DDC0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DDRC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DDM</td>
</tr>
<tr>
<td>DDC7</td>
<td>DDC6</td>
<td>DDC5</td>
<td>DDC4</td>
<td>DDC3</td>
<td>DDC2</td>
<td>DDC1</td>
<td>DDC0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DDRD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DDRD</td>
</tr>
<tr>
<td>PE7</td>
<td>PE6</td>
<td>PE5</td>
<td>PE4</td>
<td>PE3</td>
<td>PE2</td>
<td>PE1</td>
<td>PE0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PORTF</td>
</tr>
<tr>
<td>FOC1</td>
<td>FOC2</td>
<td>FOC3</td>
<td>FOC4</td>
<td>FOC5</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CPOC</td>
</tr>
<tr>
<td>OC1M7</td>
<td>OC1M6</td>
<td>OC1M5</td>
<td>OC1M4</td>
<td>OC1M3</td>
<td>--</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OC1M</td>
</tr>
<tr>
<td>OC1D7</td>
<td>OC1D6</td>
<td>OC1D5</td>
<td>OC1D4</td>
<td>OC1D3</td>
<td>--</td>
<td>--</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OC1D</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>Bit 15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>Bit 8</td>
</tr>
<tr>
<td>Bit 7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>Bit 0</td>
</tr>
</tbody>
</table>
* Configure
  LDAA #$0F
  STAA $1007

* Drive PC1 High and PC3 Low
  LDAA #$02
  STAA $1003

* Read Inputs (High nibble only)
  LDAA $1003
Digital I-O Considerations

- Electrical Characteristics and Limitations
- Alternative Functions
  - Chip Level
  - Board Level
- Electrical Type
  - Straight CMOS/TTL
  - Flip-Flop / Schmitt
  - Open-Collector / Open-Drain
Memory or Input /Output Mapping

• Memory I/O
  – LDAA #$01 ; turn on bit 0
  – STAA $1003 ; output to port C

• Other Processors have separated I/O and memory space
• They have special instruction for I/O
  – IN (Port #)
  – OUT (data, Port#)
• (Motorola use same Memory space)
Electrical Interfaces 1

- Digital Output-Only Pin
- Minimum $V_{OH} = V_{DD} - 0.8V$ @ 0.8 mA
- Maximum $V_{OL} = 0.4V$ @ 1.6 mA
- Maximum $I_{OUT} = 25$ mA

Figure 2-19. Internal Circuitry — Output-Only Pin
Electrical Interfaces 2

- Digital Input-Only Pin
- CMOS Buffer
- Minimum $V_{IH} = 0.7 \times V_{DD}$
- Maximum $V_{IL} = 0.2 \times V_{DD}$

![Figure 2-15. Internal Circuitry — Digital Input-Only Pin](image-url)
Electrical Interfaces 3

- Analog Input-Only Pin (PE0-7)
- Minimum $V_{\text{in}} = -0.3 \text{ V}$
- Maximum $V_{\text{in}} = V_{\text{DD}} + 0.3\text{V}$

Figure 2-16. Internal Circuitry — Analog Input-Only Pin
Electrical Interfaces 4

- Digital I-O Pin
- Totem-Pole Output
- CMOS Input

Figure 2-17. Internal Circuitry — Digital I/O Pin
Electrical Interfaces 5

- Digital I-O Pin
- Open-Drain Output
- CMOS Input

PORTC and PORTD can do this.

Figure 2-18. Internal Circuitry — Input/Open-Drain-Output Pin
Pin Logic - Components

- PROTECTION
- THICK-FIELD PROTECTION DEVICE
- TRANSMISSION GATE
- [3] — REFERENCE NUMBER
- DDRA7 — CONTROL BIT
Pin Logic 1 (PA0 – PA2)

Figure 7-4. PA2–PA0 (IC3–IC1) Pin Logic
Pin Logic 2 (Port B)

Figure 7-8. Port B Pin Logic
Pin Logic 3 (PA3 – PA6)
Digital I-O Gotchas

1. Current Sink/Source Capability
2. Voltage Level Capability
   - THESE ARE INTER-RELATED
3. External Hardware Compatibility
4. Signal Timing
A simple example

```
Configure
LDAA #$0F
STAA $1007

Drive PC1 High and PC3 Low
LDAA #$02
STAA $1003

Read Inputs (High nibble only)
LDAA $1003
```
Controlling a Display
Controlling a Display

Figure 9.5: Parallel Output A

(a) Common Anode Example

Hex Code = 0101

(b) Common Cathode Example

Hex Code = 0110
Controlling a Display