The following text is taken directly from the 68HC11 Reference Manual. It is to accompany slides 17 - 19 in the Digital I-O Lecture.

**Pin Logic 1: PA2–PA0 (IC3–IC1) Pin Logic**

Refer to Figure 7-4 for the following discussion. The cross-coupled NAND circuit with four associated inverters is a hysteresis buffer. Hysteresis is provided by sizing inverter [1] so its switch point is higher than normal and by sizing inverter [2] so its switch point is lower than normal.

Starting with 0 on the pin, a slowly rising signal causes inverter [2] to switch so that the R signal goes to an inactive-high state. As the input continues to rise, inverter [1] switches, causing a low S, which causes the cross-coupled NAND latch to set Q high and clear Q low. The low Q reinforces the S signal so that, even if noise causes inverter [1] to switch back to S = 1, the cross-coupled latch will not reset.

Conversely, starting with 1 on the pin, a slowly failing signal causes inverter [1] to switch, causing the S signal to be placed in an inactive-high state. As the input continues to fall, inverter [2] switches, causing a low R. This low R resets the cross-coupled NAND latch, setting Q high and clearing Q low. The low Q reinforces the R signal so that, even if noise causes inverter [2] to switch back to R = 1, the cross-coupled latch will not become set.

For bits 0, 1, and 2, port A reads return the buffered states of the corresponding pins. Port A reads are completely independent of timer input-capture functions.

**Pin Logic 2: Port B Pin Logic**

Refer to Figure 7-8 for the following discussion. Reads of port B return the logic state from a point inside the output pin buffer. During reads of port B, transmission gate [1] is enabled by the RPORTB signal to couple logic state [2] to the internal data bus. The RPORTB signal is not asserted for port B reads in expanded modes since port B is an external address in that case.

In single-chip modes, the mode A (MDA) control bit is 0, which enables AND gate [3] and disables AND gate [4]. The internal data bus is coupled through AND gate [3] and clocked into HFF [5] by the write port B (WPORTB) signal. The output of HFF [5] is buffered and driven out the port B pins. In single-chip modes, HFF [5] is set to 1 by AND gate [6] during reset, which results in logic 0 at the port B pins.

In expanded modes, the MDA control bit is 1, enabling AND gate [4] and disabling AND gate [3], which couples high-order addresses to HFF [5]. In expanded modes, HFF [5] is transparent while address strobe (AS) is high and latched while AS is low. The output of HFF [5] is buffered and driven out the port B pins.
Pin Logic 3: PA6–PA3 (OC5–OC2) Pin Logic

Refer to Figure 7-5 for the following discussion. For bits 3, 4, 5, and 6, port A reads return the logic state from a point inside the output pin buffer. During a port A read, transmission gate [1] is enabled to couple the logic state at the input of inverter [2] to the internal data bus.

Inverter [2] is driven by a head-to-tail cheater latch. The feedback inverter [3] in this cheater latch is sized to be overridden by transmission gate [4], [5], or [6]. These three transmission gates correspond to the three possible sources of data for these port A pins as follows.

General-purpose port A outputs come through transmission gate [4] from HFF latch [7]. Output compares 5 through 2 (OC5–OC2) affect their corresponding port A pin via transmission gate [6]; output compare 1 (OC1) can affect these port A pins via transmission gate [5].

Control gate [8] enables general-purpose port A outputs during PTACLK when no timer function is enabled to control this pin. PTACLK is an internal clock signal that synchronizes port A pin changes to the falling edge of E. OC1 is enabled when the corresponding OC1Mx bit is 1, which disables control gate [8] and enables control gate [9]. The OC5–OC2 functions are enabled to control their corresponding port A pin by the OMx:OLx bits not equal to 0:0. When OMx:OLx are not 0:0, control gate [8] is disabled and control gate [10] is enabled.

Control gate [9] allows OC1 to affect this port A pin. When the corresponding OC1Mx control bit is 1, control gate [9] is enabled. The PTACLK clock signal acts as a strobe. When there is a successful OC1 compare (OC1CMP) or when OC1 is forced by FOC1 equals 1, control gate [9] enables transmission gate [5], which causes the corresponding OC1Dx state to be transferred to cheater latch [3]. NAND gate [11] provides a disable to control gate [10] so that if OC1 and another output compare simultaneously attempt to change the same port A pin, OC1 will override.

Control gate [10] is enabled by the corresponding OMx:OLx control bits not equal to 0:0. When there is a successful output compare x (OCxCMP) or when OCx is forced by FOCx equals 1, control gate [10] enables transmission gate [6] and momentarily disables transmission gate [12]. Transmission gate [12] transfers the previous port A pin state to cheater latch [14]. Cheater latch [14] holds the previous pin state stable for logic [13] while transmission gate [12] is disabled and transmission gate [6] is enabled. Set-reset (S/R) latch [13] and associated logic is used to determine the next timer output state that would result from a successful OCx compare. This next timer output state is determined by the states of the associated OMx and OLx control bits and the previous port A pin state.