Analog I/O
Analog I/O

- **A/D**

- **D/A**
Min and Max

• ADC levels defined with respect to two pins:
  – VRH (Pin 52) sets the high reference voltage
  – VRL (Pin 51) sets the low reference voltage
  – Resolution specified by the # of bits in the result (8)

• On the EVBPlus2, tied to VDD and VSS through J11.
  – VRH = VDD = 5V
  – VRL = VSS = 0v
  – RANGE = 5V
  – RESOLUTION = 5v / 2^8 = 19.5 mV / bit
<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Parameter</th>
<th>Min</th>
<th>Absolute</th>
<th>2.0 MHz</th>
<th>3.0 MHz</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>Number of Bits Resolved by A/D Converter</td>
<td>---</td>
<td>8</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Non-Linearity</td>
<td>Maximum Deviation from the Ideal A/D Transfer Characteristics</td>
<td>---</td>
<td>---</td>
<td>± 1/2</td>
<td>± 1</td>
<td>LSB</td>
</tr>
<tr>
<td>Zero Error</td>
<td>Difference Between the Output of an Ideal and an Actual for Zero Input Voltage</td>
<td>---</td>
<td>---</td>
<td>± 1/2</td>
<td>± 1</td>
<td>LSB</td>
</tr>
<tr>
<td>Full Scale Error</td>
<td>Difference Between the Output of an Ideal and an Actual A/D for Full-Scale Input Voltage</td>
<td>---</td>
<td>---</td>
<td>± 1/2</td>
<td>± 1</td>
<td>LSB</td>
</tr>
<tr>
<td>Total Unadjusted Error</td>
<td>Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error</td>
<td>---</td>
<td>---</td>
<td>± 1/2</td>
<td>± 1 1/2</td>
<td>LSB</td>
</tr>
<tr>
<td>Quantization Error</td>
<td>Uncertainty Because of Converter Resolution</td>
<td>---</td>
<td>---</td>
<td>± 1/2</td>
<td>± 1/2</td>
<td>LSB</td>
</tr>
<tr>
<td>Absolute Accuracy</td>
<td>Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included</td>
<td>---</td>
<td>---</td>
<td>± 1</td>
<td>± 2</td>
<td>LSB</td>
</tr>
<tr>
<td>Conversion Range</td>
<td>Analog Input Voltage Range</td>
<td>$V_{RL}$</td>
<td>$V_{RH}$</td>
<td>$V_{RH}$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{RH}$</td>
<td>Maximum Analog Reference Voltage (Note 2)</td>
<td>$V_{RL}$</td>
<td>---</td>
<td>$V_{DD} + 0.1$</td>
<td>$V_{DD} + 0.1$</td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{RL}$</td>
<td>Minimum Analog Reference Voltage (Note 2)</td>
<td>$V_{SS} - 0.1$</td>
<td>---</td>
<td>$V_{RH}$</td>
<td>$V_{RH}$</td>
<td>$V$</td>
</tr>
<tr>
<td>$\Delta V_R$</td>
<td>Minimum Difference between $V_{RH}$ and $V_{RL}$ (Note 2)</td>
<td>3</td>
<td>---</td>
<td></td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>Conversion Time</td>
<td>Total Time to Perform a Single Analog-to-Digital Conversion:</td>
<td>---</td>
<td>32</td>
<td>$t_{cyc} + 32$</td>
<td>$t_{cyc} + 32$</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>a. E Clock</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>b. Internal RC Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Monotonicity</td>
<td>Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Zero Input Reading</td>
<td>Conversion Result when $V_{in} = V_{RL}$</td>
<td>00</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>Hex</td>
</tr>
<tr>
<td>Full Scale Reading</td>
<td>Conversion Result when $V_{in} = V_{RH}$</td>
<td>---</td>
<td>---</td>
<td>FF</td>
<td>FF</td>
<td>Hex</td>
</tr>
<tr>
<td>Sample Acquisition Time</td>
<td>Analog Input Acquisition Sampling Time:</td>
<td>---</td>
<td>12</td>
<td>---</td>
<td>12</td>
<td>$\mu s$</td>
</tr>
<tr>
<td></td>
<td>a. E Clock</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>b. Internal RC Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample/ Hold Capacitance</td>
<td>Input Capacitance during Sample PE0-PE7</td>
<td>20 (Typ)</td>
<td>---</td>
<td>---</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Input Leakage on A/D Pins PE0-PE7</td>
<td>$V_{RL}$, $V_{RH}$</td>
<td>---</td>
<td>400</td>
<td>400</td>
<td>nA</td>
</tr>
</tbody>
</table>
Analog Input

- The 68HC11 has analog input only (eight 8-bit channels)
- These channels accept voltages in the range 0 – 5 Volts only
- What if your sensor produces voltages in the -5 to +5 Volt range?
- Or – What if your signal does not have enough current to trigger the A/D conversion properly
Signal Conditioning

(a) Inverting Amplifier

\[ V_{\text{out}} = \frac{-R_f}{R_i} V_{\text{in}} \]

(b) Noninverting Amplifier

\[ V_{\text{out}} = \frac{R_f + R_i}{R_i} V_{\text{in}} \]

(c) Differential Amplifier

\[ V_{\text{out}} = \frac{-R_f (V_1 - V_2)}{R_i} \]

(d) Summing Amplifier

\[ V_{\text{out}} = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \]
Port

• Analog Input uses Port E (PE0 – PE7)
  – Port E can be used for mixed-signal I/O
  – Not recommended if avoidable

• Eight 8-bit analog inputs
  – Single A/D converter
  – 8-way analog multiplexer

• Is a *successive approximation* type A/D converter
Successive Approximation A/D

(a) Block Diagram of Successive-Approximation System

- $V_{IN}$ from an analog sample and hold circuit
- $V_{OUT}$ from a DAC
- Comparator
- Digital Output
- Done Conversion
- Logic
- $C_{OUT}$ high if $V_{IN} > V_{OUT}$
- $C_{OUT}$ low if $V_{IN} \leq V_{OUT}$

Thursday, 21 March 13
Analog I/O
Successive Approximation Example

• Assume a 4-bit ADC
• Let:
  – VRH = 4V
  – VRL = 0V
  – Resolution = 4 / 2^4 = 0.25 V

• Input Voltage = 2.25V
• Input Voltage = 1.75V
• Input Voltage = 1.80V
Successive Approximation Example

\[ V_{IN} \]

\[ + \]

\[ - \]

DAC

ADC Logic

ADRES

3 | 2 | 1 | 0
2.25V - Step 1

2.25 V

+ 1

- 1

2.00 V DAC

1 | 0 | 0 | 0

ADR

ADC Logic

ADR [3] = 1
2.25V - Step 2

2.25 V

+ -

0

3.00 V DAC

1 | 1 | 0 | 0

ADR

ADR [2] = 0

ADC Logic
2.25V - Step 3

ADR [1] = 0
2.25V - Step 4

ADR [0] = 1

Analog I/O

Thursday, 21 March 13
1.75V - Step 1

1.75 V

2.00 V
DAC

1 | 0 | 0 | 0
ADR

ADC Logic

0

ADR [3] = 0
1.75V - Step 2

1.75 V

+ 1

- ADR [2] = 1

1.00 V DAC

0 | 1 | 0 | 0

ADC Logic
1.75V - Step 3

1.75 V

1.50 V
DAC

0 | 1 | 1 | 0
ADR

+ -

1

ADC
Logic

ADR [1] = 1
1.75V - Step 4

1.75 V

+ 1

- 1

1.75 V DAC

0 | 1 | 1 | 1

ADR

ADC Logic

ADR [0] = 1
Operation

(a) Sample Mode

(b) Hold Mode

MSB | LSB
--- | ---
SUCCESSIVE APPROXIMATION REGISTER (SAR)
Figure 12-5. Timing Diagram for a Sequence of Four A/D Conversions
Alternative ADC Topologies

• Successive Approximation
  – Conversion time constant regardless of voltage
  – In the HC11, 32 e-clock cycles

• Ramp ADC
  – Conversion time proportional to voltage
  – Old-school technique, saved on chip footprint space.

• Flash ADC
  – Conversion time = 1 clock cycle
  – Fastest but most footprint and power intensive.
Initialisation

- The 68HC11 A/D subsystem is OFF after power-on or reset
- You must therefore turn it ON before using it
- To do this, set the A/D Power Up bit (ADPU) in the configuration options (OPTION) register
- Also, select the E-clock as the clock source by setting the clock select bit (CSEL) in the OPTION register
68HC11 Oddities

- The 68HC11 performs A/D conversions in batches of 4

- You can sample 1 channel 4 times, or sample a bank of 4 channels once

- This is selected with the multichannel control (MULT) bit in the A/D control (ADCTL) register
Single Channel

- Set bit MULT to zero
- Set SCAN bit in ADCTL to zero to perform a single conversion – set to 1 for continuous conversions
- Set Bits CC, CB and CA to select channel to convert
- Wait for conversion complete flag (CCF) to be set
- Read result from any of the A/D result registers (ADR1 – ADR4)
<table>
<thead>
<tr>
<th>CD</th>
<th>CC</th>
<th>CB</th>
<th>CA</th>
<th>Channel Signal</th>
<th>Result in ADRx If MULT = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>PE0</td>
<td>ADR1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>PE1</td>
<td>ADR2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>PE2</td>
<td>ADR3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>PE3</td>
<td>ADR4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>PE4*</td>
<td>ADR1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>PE5*</td>
<td>ADR2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>PE6*</td>
<td>ADR3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PE7*</td>
<td>ADR4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
<td>ADR1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
<td>ADR2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Reserved</td>
<td>ADR3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td>ADR4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$V_H^{**}$</td>
<td>ADR1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$V_L^{**}$</td>
<td>ADR2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$1/2 V_H^{**}$</td>
<td>ADR3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td>ADR4</td>
</tr>
</tbody>
</table>

*Not available in 48-pin package versions
**These channels intended for factory testing
Multi Channel

- Set bit MULT to one

- Set SCAN bit in ADCTL to zero to perform a single conversion – set to 1 for continuous conversions

- Set Bits CD and CC to select channels to convert (CB / CA have no effect)

- Wait for conversion complete flag (CCF) to be set

- Read result from the A/D result registers (ADR1 – ADR4)
<table>
<thead>
<tr>
<th>CD</th>
<th>CC</th>
<th>CB</th>
<th>CA</th>
<th>Channel Signal</th>
<th>Result in ADRx If MUL T = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>PE0</td>
<td>ADR1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>PE1</td>
<td>ADR2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>PE2</td>
<td>ADR3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>PE3</td>
<td>ADR4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>PE4*</td>
<td>ADR1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>PE5*</td>
<td>ADR2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>PE6*</td>
<td>ADR3</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PE7*</td>
<td>ADR4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
<td>ADR1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
<td>ADR2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Reserved</td>
<td>ADR3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td>ADR4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>$V_H^{**}$</td>
<td>ADR1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$V_L^{**}$</td>
<td>ADR2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$1/2 V_H^{**}$</td>
<td>ADR3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved**</td>
<td>ADR4</td>
</tr>
</tbody>
</table>

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**These channels intended for factory testing