The Bus/Tristate
Bus Review

• The Bus is simply a set of parallel signal lines

• The Bus connects the microcontroller unit (MCU) to other devices

• The MCU receives power and clock signals through the bus

• To select a device, an address is sent on the address bus

• Data is then communicated over the data bus
Bus Diagram

MCU = Microcontroller Unit
PRU = Port Replacement Unit
RAM = Random Access Memory
EPROM = Erasable Programmable Read-Only Memory
COM = Communications Port
Tristate

• For the MCU to use a device, it must enable the device

• The MCU can also disable devices on the bus

• To disable a device means that it is disconnected from the bus

• Tristate devices have 3 possible states, logic high, logic low and high impedance

• When a device is in high impedance mode, it is said to be ‘tristated’
Tristate

• When a device is tristated, it is effectively disconnected from the bus

• Only one device on a bus should be enabled at any one time
Figure 5.2  Tristate Analogy Using Mechanical Switches (Z = High Impedance)
Tristate Logic

Note: $Z = \text{High Impedance}$

**Figure 5.3** Tristate Logic
Tristate Logic

V_{CC}

VALUE
ENABLE
I/O PIN
Control Lines

• When E is low, a device is enabled

• If a device can be written to and read from, R/W determines the direction of data – if low, data is written to the chip, if high, data is read

• The clock signal G synchronises any data transfer (this is the E-clock on the EVBPlus)
An Example

[Diagram of a memory chip and MCU or Other Device connection with address lines A0 to A12, data lines D0 to D7, enable (E), read/write control (W), and clock (C).]
Address Decoding

• How do we only enable the chip we are addressing, and no others?

• The signals on the address bus determine which location is addressed

• Many chips (memory etc.) use only a subset of address lines (previous example) because they occupy only a subset of address space

• The extra bits on the address line can be used to determine which chip needs to be enabled
Address Decoding 2

• An Example: any address in the range $2000 to $3FFF (8Kb) has the same value for the top three address bits A15,A14,A13 (%001)

• In this example, these bits can be used to determine which chip is enabled

• An address decoder chip (such as the 74HC138) can be used to select 1 of 8 eight Kilobyte devices

• If the device is smaller than 8Kb, some address space may be wasted
Address Decoder

(a) Logic Diagram

(b) Function Table

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<thead>
<tr>
<th>Chip Select Conditions</th>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS1 = 1</td>
<td>A2 A1 A0</td>
<td>Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7</td>
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<tr>
<td>CS2 = 0</td>
<td>0 0 0</td>
<td>0 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>CS3 = 0</td>
<td>0 0 1</td>
<td>1 0 1 1 1 1 1 1</td>
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Figure 5.5 74HC138
1-of-8 Decoder
Bus Architecture Summary

- Devices only drive their outputs if selected and set to write
- Tristated devices can still read the bus
- Address Decoding enables multiple small devices to share a large memory space without conflict
- All devices have Address, Data, R/W and Clock lines in common. (CS is the only differentiated line)