Timing Diagrams
Timing Diagrams

- Timing Diagrams show how signals change with time
- Time is on the horizontal axis (as usual)
- The signal(s) are on the vertical axis
Timing Diagram Formats

(a) Single Bit (Line) Timing Diagram

(b) Bus Timing Diagram
Figure 10-35. Output-Compare Timing Details
Timing Specifications

Figure 7.3 Clock Details and Port Read Timing (f = 2 MHz)
example

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Note: Measurement points are 20% and 70% of \( V_{DD} \).
Clocking

- The clock signal is a periodic series of pulses
- In the 68HC11, when the clock is low, an internal process is taking place
- When the clock is high, the MCU is writing or reading data
- Divide-by-Four forms an integral part of the clocking system.
68HC11 Internal Clocks

Figure 10-3. Timing Summary for Oscillator Divider Signals
Bus Timing for Data Write Cycle

- **Bus Timing** for Data Write Cycle

- **MCU** puts data on bus during write cycle
- **MCU** reads data during read cycle

- **E Clock**

- **R/W Write Operation**

- **Port B Address High Byte**

- **Port C Multiplexed Address Low Byte/ Data**

- **Previous Data Byte**
- **Address Low Byte**
- **Data Byte**

- **AS Address Strobe**
Bus Timing for Data Write Cycle
Expanded Multiplexed Mode

- Port B has high byte of address
- Port C has low byte of address and then a byte of data
  - Address Strobe (AS) forms part of the control bus, it is asserted (held high) when an address is available
  - AS is used by external hardware to demultiplex signals

- Address is guaranteed to be valid on the E-clock rising edge.
- Data is transferred on the E-clock falling edge.
Memory Access R/W

(a) Read Operation
MCU reads data from a selected address, example $5754.

(b) Write Operation
MCU writes data to a selected address, example $2754.

Note:
- Data Bus is bidirectional.
- MCU writes data when Clock goes high.
- MCU reads data when Clock goes from high to low.
Common Timing Diagrams

• Clock Scheduling

• Serial Transactions

• Timer/Counter behaviour

• Digital I/O Specification/Limits
Example 1: 1110 (qualifier), then two zeros out of 3
Figure 9-15. Start Bit — Noise Case Five
Example 3

Figure 10-32. Timer Counter as MCU Leaves Reset

Figure 10-33. Timer Counter Read — Cycle-by-Cycle Analysis
Timing

Figure 7.3 Clock Details and Port Read Timing (E = 2 MHz)

Figure 10-32. Timer Counter as MCU Leaves Reset

$^*$ Sequence is the same for any reset (external, COP, or clock monitor) and any mode (normal or special).

Figure 10-33. Timer Counter Read — Cycle-by-Cycle Analysis
Figure 10-35. Output-Compare Timing Details