68HC11 Review
68HC11 Component Systems

- CPU
- ALU
- Memory Map
- Operating Modes
- Interrupt System
- Digital I/O
- Analog/Digital Converter
- Synchronous Serial I/O
- Asynchronous Serial I/O
- Timer Subsystem
68HC11 CPU

- 8-Bit Core

- Most Opcodes (with operand) are longer than 8-bit.

- Most Opcodes have multiple addressing modes

- Opcode specifies operation as-well as mode

- C.C.R. acts as base for conditional branches
68HC11 ALU

• Native 8-bit (Add, Subtract, Multiply)

• Microcoded 16-Bit divides

• Working in more than 8-bits = slow
• Divides = slow
• No native floating point support = EXTREMELY slow

• *C compiler can hide complexity, but doesn’t make things any faster.*
68HC11 Memory Map

• 8-bit data bus
  – Almost all memory locations are 8-bits wide

• 16-bit address bus
  – Loose 0x40 bytes to registers
  – Loose some space to stack (unspecified...)
  – Loose some space to programme

• Extremely limited internal resources
  – 256 bytes RAM
  – 8K ROM

• Expanded multiplexed mode enables extension

• Some integrated protections (64 E-cycle lockouts)
68HC11 Operating Modes

• Single-Chip
  – Potentially more reliable
  – Much less capable

• Expanded Multiplexed
  – More components to fail = less reliable
    • External Address Demultiplexer – 74HC573N
    • Port Replacement Unit (PRU) – 68HC24
  – Much more capable

• Bootstrap & Special Test Modes
  – Special purpose use ONLY
68HC11 Interrupt System

- Interrupts triggered by logical AND:
  - Local Flag & Local Mask & Global Mask
- When an interrupt is triggered, ISR address fetched from the IVT
  - Many interrupt vectors, some are shared.
- An ISR Should:
  - Clear it’s own flag bit
  - Handle the interrupt
  - BE SHORT
68HC11 Digital I/O

- 5 Ports – 38 Bits
- Mixture of I/O, I and O
- PORTC and PORTB used in expanded multiplexed
  – 68HC24 PRU replaces them exactly as they were
- I/O ports MUST be configured appropriately
68HC11 ADC

• 8-Bit ADC – Sec. 7
  – 0x00 = \( V_{RL} \) (=0V)
  – 0xFF = \( V_{RH} \) (=5V)

• 8 input channels, 4 conversions/batch
  – Single channel – 4 sequential conversions
  – Multi-channel – 4 ‘simultaneous’ conversions

• Scan mode sacrifices power for availability
  – Can cause issues at v. high frequencies

• *Conversions NOT instantaneous* (Fig 7-1)
68HC11 Asynchronous Serial

• SCI – Sec. 5
• Asynchronous serial:
  – Match clock frequencies but not clocks
  – SCI handles clocking as per configuration
  – Baud = bits per second (don’t forget start/stop bits)
• RS232 specifies ±15V typical
  – 68HC11 is a TTL device
  – MAX232 level shifter
• *Handshaking/Error checking not done in H/W*
68HC11 Synchronous Serial

• SPI – Sec. 6

• Higher speed than SCI
• More complex to manage
• Independent of SCI

• Used for debugger on EVBPlus2
• Otherwise only of academic interest
68HC11 Timers

• 16-bit master timer TCNT
  – Prescaler bits in TMSK1
• Output Compares
  – Timer Matches → Output Actions
• Input Captures
  – Input Actions → Time Recorded

• Requires interrupt to be effective
  – Unless you’re incredibly tricky...
68HC11 Summary

- You should now be able to:
  - Write code to appropriately use ALL subsystems (except SPI)
  - Understand external hardware requirements for ALL subsystems
  - Understand the operation and capabilities of ALL subsystems
  - Interpret datasheets for ICs and µPs beyond the 68CH11

IF IN DOUBT, ASK!!!
68HC11 Summary

- Some other technical skills:
  - Make Design Decisions
  - Understand requirements for interfacing (HW & SW)
  - Back-of-the-envelope calculation
    - Storage Requirements
    - Timer Resolution & Limits
    - A/D Sample Rates
    - Serial Data Rates
  - Internal design of modules on the HW to SW boundary (Driver layer)