Applications
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- Lead-Free

Benefits
- Very Low RDS(on) at 4.5V VGS
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DS Draining Source Voltage</td>
<td>30 V</td>
<td></td>
</tr>
<tr>
<td>V_GS Gate-to-Source Voltage</td>
<td>± 20 V</td>
<td></td>
</tr>
<tr>
<td>I_D @ T_C = 25°C Continuous Drain Current, V_GS @ 10V</td>
<td>160 A</td>
<td></td>
</tr>
<tr>
<td>I_D @ T_C = 100°C Continuous Drain Current, V_GS @ 10V</td>
<td>113 A</td>
<td></td>
</tr>
<tr>
<td>I_DM Pulsed Drain Current @ 10°C</td>
<td>640 A</td>
<td></td>
</tr>
<tr>
<td>P_D @ T_C = 25°C Maximum Power Dissipation @ 10°C</td>
<td>135 W</td>
<td></td>
</tr>
<tr>
<td>P_D @ T_C = 100°C Maximum Power Dissipation @ 10°C</td>
<td>68 W</td>
<td></td>
</tr>
<tr>
<td>Linear Derating Factor</td>
<td>0.90 W/°C</td>
<td></td>
</tr>
<tr>
<td>T_J Operating Junction and Storage Temperature Range</td>
<td>-55 to +175 °C</td>
<td></td>
</tr>
<tr>
<td>T_STG Soldering Temperature, for 10 seconds</td>
<td>300 (1.6mm from case)</td>
<td></td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_JUC Junction-to-Case</td>
<td></td>
<td>1.11</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_JUA Junction-to-Ambient (PCB Mount)</td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>R_JUA Junction-to-Ambient</td>
<td></td>
<td>110</td>
<td></td>
</tr>
</tbody>
</table>

Notes: © through ® are on page 11

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Static @ $T_J = 25^\circ C$ (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BVDSS$</td>
<td>30</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{DS} = 0V, I_D = 250\mu A$</td>
</tr>
<tr>
<td>$\Delta BVDSS/\Delta T_J$</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>mV/$^\circ C$</td>
<td>Reference to $25^\circ C$, $I_D = 1mA$</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>2.4</td>
<td>3.1</td>
<td>—</td>
<td>m$\Omega$</td>
<td>$V_{GS} = 10V, I_D = 25A$</td>
</tr>
<tr>
<td></td>
<td>3.0</td>
<td>3.9</td>
<td>—</td>
<td>m$\Omega$</td>
<td>$V_{GS} = 4.5V, I_D = 20A$</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>1.35</td>
<td>1.9</td>
<td>2.35</td>
<td>V</td>
<td>$V_{DS} = V_{GS}, I_D = 100\mu A$</td>
</tr>
<tr>
<td>$\Delta V_{GS(th)/\Delta T_J}$</td>
<td>—</td>
<td>—</td>
<td>-6.4</td>
<td>mV/$^\circ C$</td>
<td></td>
</tr>
<tr>
<td>$I_{oss}$</td>
<td>—</td>
<td>—</td>
<td>150</td>
<td>nA</td>
<td>$V_{GS} = 20V$</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA</td>
<td>$V_{GS} = -20V$</td>
</tr>
<tr>
<td>$gfs$</td>
<td>89</td>
<td>—</td>
<td>—</td>
<td>S</td>
<td>$V_{GS} = 15V, I_D = 20A$</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>39</td>
<td>59</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>$Q_{gs1}$</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>nC</td>
<td>$V_{DS} = 15V$</td>
</tr>
<tr>
<td>$Q_{gs2}$</td>
<td>3.9</td>
<td>—</td>
<td>—</td>
<td>nC</td>
<td>$V_{DS} = 4.5V$</td>
</tr>
<tr>
<td>$Q_G$</td>
<td>13</td>
<td>—</td>
<td>—</td>
<td>nC</td>
<td>$I_D = 20A$</td>
</tr>
<tr>
<td>$Q_{gdr}$</td>
<td>12</td>
<td>—</td>
<td>—</td>
<td>nC</td>
<td>See Fig. 16</td>
</tr>
<tr>
<td>$Q_{sw}$</td>
<td>17</td>
<td>—</td>
<td>—</td>
<td>nC</td>
<td>$V_{DS} = 16V, V_{GS} = 0V$</td>
</tr>
<tr>
<td>$R_G$</td>
<td>0.85</td>
<td>1.5</td>
<td>—</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$t_{d(on)}$</td>
<td>19</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>$V_{DD} = 15V, V_{DS} = 4.5V$</td>
</tr>
<tr>
<td>$I_t$</td>
<td>35</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>$I_D = 20A$</td>
</tr>
<tr>
<td>$t_{d(off)}$</td>
<td>21</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>$R_G = 1.8\Omega$</td>
</tr>
<tr>
<td>$t_f$</td>
<td>17</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>See Fig. 14</td>
</tr>
<tr>
<td>$C_{iss}$</td>
<td>4880</td>
<td>—</td>
<td>—</td>
<td>pF</td>
<td>$V_{DS} = 0V$</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>950</td>
<td>—</td>
<td>—</td>
<td>pF</td>
<td>$V_{DS} = 15V$</td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>470</td>
<td>—</td>
<td>—</td>
<td>pF</td>
<td>$f = 1.0MHz$</td>
</tr>
</tbody>
</table>

### Avalanche Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{AS}$</td>
<td>—</td>
<td>250</td>
<td>mJ</td>
</tr>
<tr>
<td>$I_{AR}$</td>
<td>—</td>
<td>20</td>
<td>A</td>
</tr>
<tr>
<td>$E_{AR}$</td>
<td>—</td>
<td>13.5</td>
<td>mJ</td>
</tr>
</tbody>
</table>

### Diode Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>—</td>
<td>—</td>
<td>160</td>
<td>A</td>
<td>MOSFET symbol showing the integral reverse p-n junction diode.</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>—</td>
<td>—</td>
<td>640</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$V_{SD}$</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>V</td>
<td>$T_J = 25^\circ C, I_S = 20A, V_{DS} = 0V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>—</td>
<td>18</td>
<td>27</td>
<td>ns</td>
<td>$T_J = 25^\circ C, I_F = 20A, V_{DD} = 15V$</td>
</tr>
<tr>
<td>$Q_r$</td>
<td>—</td>
<td>32</td>
<td>48</td>
<td>nC</td>
<td>$di/dt = 3000\mu A/\mu s$</td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)</td>
</tr>
</tbody>
</table>
**Fig 1.** Typical Output Characteristics

**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics

**Fig 4.** Normalized On-Resistance vs. Temperature
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area
**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Threshold Voltage vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case
IRLR/U8743PbF

**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Fig 13.** Gate Charge Test Circuit

**Fig 14a.** Switching Time Test Circuit

**Fig 14b.** Switching Time Waveforms
Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

• dv/dt controlled by \( R_G \)
• Driver same type as D.U.T.
• \( I_{SD} \) controlled by Duty Factor “D”
• D.U.T. - Device Under Test

\[ \text{\begin{align*}
\text{Driver Gate Drive} & \quad \text{D} = \text{P.W.} \\
\text{D.U.T.} & \quad \text{D.U.T. ISD Waveform} \\
\text{Re-Applied} & \quad \text{Body Diode Forward Voltage} \\
\text{Voltage} & \quad \text{Diode Recovery dv/dt} \\
\text{Inductor Current} & \quad \text{Body Diode Forward Drop} \\
\text{Ripple} \leq 5\% & \quad V_{ISD}
\end{align*}} \]

* \( V_{GS} = 5V \) for Logic Level Devices

Fig 16. Gate Charge Waveform

\[ \text{\begin{align*}
\text{Id} & \quad \text{Vgs} \\
\text{Vds} \quad & \quad \text{Vgs(th)} \\
\text{Qgodr} & \quad \text{Qgd} \\
\text{Qgs2} & \quad \text{Qgs1}
\end{align*}} \]
Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the \( R_{ds(on)} \) of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

\[
P_{loss} = P_{\text{conduction}} + P_{\text{switching}} + P_{\text{drive}} + P_{\text{output}}
\]

This can be expanded and approximated by;

\[
P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left( I \times Q_{gs} \times V_{in} \times f \right) + \left( I \times Q_{gsv} \times V_{in} \times f \right) + \left( Q_{os} \times V_{g} \times f \right) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right)
\]

This simplified loss equation includes the terms \( Q_{gs} \) and \( Q_{os} \) which are new to Power MOSFET data sheets. \( Q_{gs} \) is a sum of elements of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, \( Q_{gsv} \) and \( Q_{gs} \), can be seen from Fig 16.

\( Q_{gs} \) indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to \( I_{\text{max}} \), at which time the drain voltage begins to change. Minimizing \( Q_{gs} \) is a critical factor in reducing switching losses in Q1.

\( Q_{os} \) is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how \( Q_{os} \) is formed by the parallel combination of the voltage dependent (non-linear) capacitance’s \( C_{os} \) and \( C_{pm} \) when multiplied by the power supply input bus voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

\[
P_{loss} = P_{\text{conduction}} + P_{\text{drive}} + P_{\text{output}}
\]

\[
P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left( Q_{gsv} \times V_{in} \times f \right) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right)
\]

\*dissipated primarily in Q1.

For the synchronous MOSFET Q2, \( R_{ds(on)} \) is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge \( Q_{oss} \) and reverse recovery charge \( Q_{rss} \) both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs’ susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and \( V_{in} \). As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of \( Q_{rss}/Q_{gsv} \) must be minimized to reduce the potential for Cdv/dt turn on.

Figure A: \( Q_{oss} \) Characteristic

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D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. Dimensions shown in inches (milimeters)
3. Lead dimension uncontrolled in L1.
5. Section C-C dimensions apply to the flat section of the lead between 0.065 and 0.100 (0.165 and 0.250) from the lead tip.
6. Dimension D & E do not include mold flash. Mold flash shall not exceed 0.005 (0.13). For Use, these dimensions are measured at the molding extremes of the plastic body.
7. Dimension A, B & C applied to base metal only.
8. Datum A & B to be determined at datum plane K.
9. Outline conforms to JEDEC outline TO-252AA.

D-Pak (TO-252AA) Part Marking Information

Example: THE IS AN IRF840
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON VW 16, 2001
IN THE ASSEMBLY LINE 99

Note: "A" in assembly line position indicates "Lead-Free"

Note: "P" in assembly line position indicates "Plastic Package"

**Note:** For the most current drawing please refer to IR website at [http://www.irf.com/package/](http://www.irf.com/package/)

www.irf.com
IRLR/U8743PbF

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

---

**I-Pak (TO-251AA) Part Marking Information**

**Example:**

THIS IS AN IRF U20
WITH ASSEMBLY
LOT CODE: 5678
ASSEMBLED ON W1 19, 2001
IN THE ASSEMBLY LINE "A"

Note: *P* in assembly line position indicates lead-free part

---

**Note:** For the most current drawing please refer to IR website at [http://www.irf.com/package/](http://www.irf.com/package/)
Rerpetitive rating; pulse width limited by max. junction temperature.

Starting T_J = 25°C, L = 1.252 mH, R_G = 25Ω, I_A = 20A.

Pulse width ≤ 400µs; duty cycle ≤ 2%.

Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 50A.

When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

NOTES: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR’s Web site.

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